AMENDMENTS

Please amend the application as follows:

In the Claims

Please cancel claims 5 and 8 without prejudice or disclaimer.

Please substitute the following clean copy text for the pending claims 1, 3, and 6.

1. (thrice amended) A transistor circuit for implementing a switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a transistor device having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a third switch node for receiving the control signal; and

an impedance circuit connected to the third switch node and the third terminal of the transistor device, the impedance circuit configured with a sufficiently high impedance to reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch.

3. (twice amended) A transistor circuit for implementing a switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

C2

a transistor device having a first terminal connected to the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal for controlling the electrical connectivity between the first terminal and the second terminal; and

an inverter circuit connected to the second terminal of the transistor device for reducing the noise at the first terminal of the transistor device, the inverter circuit configured to reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit by providing a voltage to the second terminal when the control signal engages the transistor device.

6. (twice amended) A transistor circuit for implementing a differential switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a first transistor device having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a second transistor device having a first terminal connected to the second terminal of the first transistor device, a second terminal connected to the second switch node, and a third terminal configured to receive the control signal; and

a third transistor device having a first terminal connected to the first terminal of the first transistor device, a second terminal connected to the second terminal of the second transistor device, and a third terminal configured to receive the control signal, the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit.

Please add the following ***new*** claims:

9. (new claim) The transistor circuit of claim 6, wherein the predetermined parasitic characteristics of the third transistor device reduce the effective parasitic capacitance of the transistor circuit while sustaining a less than equivalent increase in resistance of the transistor circuit.

10. (new claim) The transistor circuit of claim 6, wherein the predetermined parasitic characteristics of the third transistor device reduce the effective parasitic resistance of the transistor circuit while sustaining a less than equivalent increase in capacitance of the transistor circuit.